Non-integral event timing for digital logic simulation

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↑ ABSTRACT

Due to reasons of efficiency, digital logic simulation is normally performed by restricting timing
accuracy to integral event timing. However, this restriction causes disadvantages which can be
avoided if a sufficiently efficient event processing algorithm for nonintegral timing becomes available.
The algorithm described here combines features of the standard linear list algorithm and the time-
mapping algorithm often used for logic simulation. The combination results in a compromise between
the timing accuracy of the former and the efficiency of the latter. The control mechanism required for
the new algorithm can and should be directly exploited to improve the control and flexibility of the
detailed simulation processing. Some of the advantages gained due to non-integral timing are
described in the conclusions of this paper.

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↑ INDEX TERMS

Primary Classification:
  B. Hardware
  ↳ **B.6** LOGIC DESIGN
    ↳ **B.6.3** Design Aids
      ↳ **Subjects:** Simulation

Additional Classification:
  E. Data
  ↳ **E.1** DATA STRUCTURES
    ↳ **Subjects:** Lists, stacks, and queues

  F. Theory of Computation
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    ↳ **F.2.2** Nonnumerical Algorithms and Problems
      ↳ **Subjects:** Sequencing and scheduling

  I. Computing Methodologies
  ↳ **I.6** SIMULATION AND MODELING
    ↳ **I.6.8** Types of Simulation
      ↳ **Subjects:** Discrete event

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